

Ratish Gupta

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TECHNICAL SKILLS

HDL & Verification: Verilog, SystemVerilog, RTL & FSM Design, Datapath & Control Logic, STA, cocotb, Verilator, timing closure, AXI-S

Programming: Python (Numpy, Signal Processing), C/C++, C++17, Java

Tools: Quartus, Modelsim, Questasim, GTKWave, Git, Tcl Scripting (basics), Make

Embedded: ARM Cortex-M, UART, I2C, GPIO, multithreaded systems

Debug & Analysis: Oscilloscope, Logic Analyzer, LTspice, Pspice, Signal Integrity Analysis. Linux CLI

PROJECTS

- Parameterized Systolic Matrix Multiplication Unit (Personal Project) | SystemVerilog, cocotb** Mar 2026 — Apr 2026
- Designed parameterized 8×8 **output-stationary** INT8/INT32 systolic MAC array in SystemVerilog for transformer Q/K/V/O and FNN matmuls (verified at 4×4 and 8×8 with parameter-only changes).
 - Built a **cocotb + Verilator** verification comparing each PE accumulator with bit-precision against a Numpy reference model with 10,000 random matmuls passed at both array sizes with zero RTL changes.
 - Synthesized for Xilinx Artix-7 (XC7A100T) with 64 DSP48E1 slices and closed timing at 100MHz with 3.76ns positive slack (FMax = 160MHz, peak 12.8 GOPS (0.0128 TOPS) at 100 MHz for an 8×8 kernel excluding memory bandwidth and a 5-state AXI-Stream style wrapper.

- RTL Image Decompression Pipeline (3DQ5 Course Project) | SystemVerilog, FPGA** Oct 2025 — Nov 2025
- Designed and implemented a full FPGA-based image decoder in SystemVerilog on Altera DE1-SoC at 50 MHz, covering chroma upsampling, YCbCr to RGB Color Space Conversion, and 2D inverse DCT
 - Implemented pipelined 8-state FSM for upsampling and color-space conversion with 4 hardware-multiplexed multipliers, processing 2 pixels per 8-clock cycle
 - Debugged fixed-point rounding errors, 1-bit address overflow, and simulation-hardware mismatches through ModelSim waveform analysis and Quartus timing reports.
 - Achieved 55 MHz Fmax with positive timing slack by optimizing critical paths identified in Quartus timing analysis

- Real-Time Software-Defined Radio System (3DY4 Course Project) | C++, Python, Rpi** Feb 2026 — Mar 2026
- Implemented a real-time multithreaded FM receiver with mono/stereo audio and RDS metadata decode via a 3-thread producer-consumer pipeline.
 - Designed polyphase rational FIR resampler supporting arbitrary U/D ratios. eliminated intermediate buffer allocation, yielding measurable latency reduction on embedded hardware by **2.7x**
 - Prototyped full RDS decode chain in Python (BPF, carrier recovery, PLL, IQ demod, RRC, CDR, Manchester, differential, frame sync), then ported to C++
 - Diagnosed and resolved block-boundary CDR alignment bug in streaming clock-and-data recovery, confirmed via IQ constellation visualization

- 3D Room Scanner (2DX3 Course Project) | ARM MCU, Sensors, Embedded C, Python** Feb 2025 — Mar 2025
- Built a bare-metal C firmware on ARM Cortex-M MCU and by integrating a VL53L1X ToF sensor over I^2C with a 4-phase stepper motor for 360° room scans at 128 angular samples per revolution.
 - Improved spatial reconstruction accuracy by processing raw distance measurements into structured **3D point clouds** using Python (Numpy + Open3D).
 - Diagnosed and corrected **noise and synchronization** errors by correlating physical motion behavior with captured sensor data.

EXPERIENCE

- Bank of Montreal (BMO)** May 2025 — Aug 2025
Software Developer Intern Toronto, ON
- Developed and validated backend microservices with emphasis on correctness, structured testing, and failure-mode analysis.
 - Designed automated test frameworks raising regression coverage to 80%+, implemented edge-case validation across distribution services
 - Performed root-cause debugging across distributed systems, collaborating with cross-functional teams under production deadlines

EDUCATION

- McMaster University** 2023 — 2027
Bachelor of Computer Engineering Hamilton, ON
- Relevant Coursework:** Electronic Devices & Circuits (A), Microprocessor Systems (A), Communication Systems (A+), Signals & Systems (A), Control Systems
- Awards:** Dean's Honours List (2024) — Engineering Int'l Scholar Award — Faculty of Eng Award of Excellence — Dean's Global Distinction

IEEE ENGAGEMENT

- IEEE ISSCC 2026 — San Francisco, CA** Feb 2026
- Attended AI accelerator and Compute-in-Memory sessions on SRAM constraints, KV-cache scaling, and TOPS/W vs TOPS/mm² tradeoffs.
- IEEE SSCS PICO Chipathon 2026** May 2026 — Present
- Selected for IEEE Solid-State Circuits Society's multi-month open-source IC design contest targeting the GF180MCUD open PDK, participating in weekly mentor-led design sessions with industry IC designers, working through the full RTL-to-GDSII flow toward tape-out.